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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,241	PECK ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to RCE, Amendments and Remarks received 28 February 2006. Per Applicant's request, claims 1, 11, 13, and 33 have been amended. Claims 1-50 are pending.

Information Disclosure Statement

2. IDS received 2/28/2006 has been considered.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-50 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-59 of U.S. Patent No. 6,219,628 B1 to Kodosky et al., in view of US Patent 5,005,119 to Rumbaugh et al.

As an example, claims 1-10 of the instant application, a method version set of claims, claim a reconfigurable system comprising a programmable hardware element. A graphical user interface useable for configuring the reconfigurable system displays fixed hardware resource icons. User input specifies functions. A hardware configuration program specifies fixed hardware resources, based on the user input, deployable on the reconfigurable system, operable to perform the function. Dependent claims call for a display of proposed configurations, a type of measurement function, a control / automation / simulation system / specifying timing and triggering requirements. A hardware configuration program comprises generating a description file, a program, a HDL code, a hardware configuration program to configure the programmable hardware element / FPGA.

Dependent claim 2 calls for the icon to modify its appearance to visually indicate that resources have been allocated for use.

In reference to US Patent 6,219,628, as an example, the instant claims map to method claims 1-21. Claim 1 discloses a graphical program to configure a programmable hardware element / instrument with functions, generating a hardware description from the graphical program,

configuring the programmable hardware element and executing the measurement function. Claim 3 disclosed "receiving user input" to control the executing hardware element. Claim 7 discloses "timer/counter logic (specifying timing and triggering requirements). Claim 9 discloses converting the hardware description into a net list, and further into a hardware program file, and further used to configure the programmable hardware element. Claim 11 discloses the graphical program includes nodes (icons).

US Patent 5,005,119 to Rumbaugh et al disclosed a 'user selection' of icons on the display for use in a program. The program acknowledges the user selection by highlighting the icon (modifying the appearance of the icon) of the selected data (col. 12, lines 18-32).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Kodosky's invention using graphical programming to program configurable hardware, by including details related to modifying the appearance of an icon, as disclosed by Rumbaugh, because both applications apply to automated design environments (Rumbaugh, col. 1, line 11-CAD program, Kodosky, col. 1, lines 25-graphical program), whereas Rumbaugh provides additional visual indicators, to aid the user / developer.

Response to Arguments

4. Applicant has argued, in substance, the following:

(A) Regarding the double patenting rejection noted on page 16, last paragraph, of Remarks. Applicant has argued, references fail to teach, "displaying a graphical user interface on a display which is useable for configuring the reconfigurable system, wherein the graphical user interface displays fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources"

and

"deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources."

Examiner's Response:

Examiner disagrees. Kodosky ('628), col. 2, line 60, recites, "graphical program (graphical user interface displays)...may include other **icons which represent devices being controlled**." (emphasis added) This statement is referencing Kodosky USPN 4,901,221 (col. 2, line 24), which is incorporated by reference at col. 6, line 34. USPN 6,219,628 disclosed (col. 4, lines 11-17), "automatically generating hardware level functionality, e.g., programmable hardware...in response to a graphical program...to develop or define instrument functionality..." The instant application has defined **"fixed hardware resources" to include (Specification, page 6) "counters, timers, A/D converters, signal conditioning logic, computer interface logic, etc." and (Specification, page 32) "physical I/O resources such as analog to digital converters (ADCs), digital to analog converters (DACs), and digital lines, among others..."** (emphasis

added) Kodosky has disclosed a graphical user interface on a display, which displays fixed hardware resource icons coupled to the programmable hardware element.

Regarding the limitation: "deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources." Kodosky ('628), col. 12, lines 46-48, recite, "operates to transfer (deploy) the FPGA program file to the programmable hardware, e.g., the FPGA, to produce a programmed hardware equivalent to the graphical program." As noted above, icons representing fixed hardware resources are displayed on a graphical user interface.

Examiner disagrees that Examiner is 'speculating' (argument on page 18, line 1) as to the functionality provided by Kodosky.

See Kodosky- 4,901,221 (Abstract): " A method for programming a computer system having a display console for displaying (displaying a graphical user interface) images to control (functionality indicated) at least one of a virtual instrument and an instrument by the steps of displaying on the screen at least one first function-icon that references at least one first control module for controlling (functionality) at least one first function; displaying on the screen at least one iteration-icon that references iteration control module for controlling multiple iterations of data flow; displaying on the screen at least one first input variable-icon that references at least one first input variable..."

Examiner maintains the double patenting rejection.

(B) As Applicant has noted, page 21, 1st paragraph of Remarks, "Duncan nowhere discloses a reconfigurable system comprising a programmable hardware element and one or more fixed hardware resources coupled to the programmable hardware element." Applicant argues that Duncan fails to mention 'fixed hardware resources.'

Examiner's Response:

As noted in the rejection of claim 1 below, Duncan disclosed a computer aided design for programming programmable integrated circuits. Duncan disclosed a schematic component library. Page 3, line 13, "Schematic diagrams are descriptions of the physical components and interconnections of a circuit." Page 4, lines 1-5, "A schematic component is comprised of two parts: a schematic symbol (icon) which is displayed on a video monitor, and an underlying circuit design (fixed hardware resource) which defines the function of the schematic component." The configurable /programmable hardware element (integrated circuits) and related schematic components are entered using a schematic capture package (Abstract), and displayed on a monitor. Applicant has defined **"fixed hardware resources"** to include (Specification, page 6) **"counters, timers, A/D converters, signal conditioning logic, computer interface logic, etc."** and (Specification, page 32) **"physical I/O resources such as analog to digital converters (ADCs), digital to analog converters (DACs), and digital lines, among others..."** (emphasis added) Examiner points to the 'underlying circuit design', which is represented as an icon, as a 'fixed hardware resource'.

(C) As Applicant has noted, page 21, 2nd paragraph of Remarks, "nowhere does Duncan disclose a graphical user interface that displays fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources."

Examiner's Response:

Duncan disclosed (page 1, lines 7-8) a computer aided (graphical user interface) design method for programming programmable integrated circuits. Duncan disclosed (page 4, line 1) a schematic component library (fixed hardware resources). Examiner contends that the schematic component library contains such components as defined by Applicant to be "fixed hardware resources." Duncan disclosed (page 11, last sentence – page 12, line 1), "Schematic components include...**counters**, registers and flip-flops." (emphasis added) Applicant has defined **"fixed hardware resources"** to include (Specification, page 6) **"counters."** (emphasis added) Applicant argues that cited text actually discloses the use of a library of icons representing simple designs for deployment to an FPGA. Examiner points to the 'underlying circuit design', which is represented as an icon, as a 'fixed hardware resource'.

(D) As Applicant has noted, page 21, 3rd paragraph of Remarks, "Neither Wenban nor Duncan discloses any method for deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources."

Examiner's Response:

As noted above, the design created by Duncan does specify 'fixed hardware resources' such as a counter. Wenban disclosed deploying the hardware configuration (page 36 #2), "A complete FPGA configuration file can be downloaded (deployed) over the network...The other message type is a command that causes the bootstrap loader to reconfigure the FPGA (specifies the use of fixed hardware resource)...The master node can download new application-specific code to be executed on the slave nodes... Page 36, #3 discloses that a slave node (on an embedded token ring network / reconfigurable system) will sample / collect / send (perform the function). Duncan disclosed (page 11, last sentence – page 12, line 1), "Schematic components include...**counters**, registers and flip-flops." (emphasis added) Applicant has defined **"fixed hardware resources"** to include (Specification, page 6) **"counters."**

(E) As Applicant has noted, page 23, last paragraph through page 24, "neither Duncan nor Wenban provides a motivation to combine."

Examiner's Response:

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both references are directed towards developing programs to configure

hardware. It is inherent that ultimately the program is deployed onto the configurable hardware. Duncan suggested deploying the configuration, (page 13, lines 10-12) "...field programmable gate arrays operable to perform the function)...are programmed in accordance with the present invention...", but Wenban provided a more specific example at page 36, 2nd & 3rd paragraphs on left, "reconfigure the FPGA using the data stored in the SRAM. The Master node can download new application-specific code to be executed on the slave nodes...The master node can download our digital oscilloscope code to the slave to perform..." Thus, Examiner contends there is a motivation to combine the references.

Examiner maintains the rejection of claims 1-50.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-21, 23-41, and 43-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 94/15311 to Duncan (hereinafter Duncan), in view of "A Software Development System for FPGA-Based Data Acquisition Systems" by Alan Wenban and Geoffrey Brown (hereinafter Wenban). (Duncan & Wenban submitted as IDS on 10/06/2004)

Per claim 1:

A method for configuring a reconfigurable system, the method comprising:

-displaying a graphical user interface on a display which is useable for configuring the reconfigurable system, wherein the reconfigurable system comprises a programmable hardware element and one or more fixed hardware resources coupled to the programmable hardware element, and wherein the graphical user interface displays fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources;

Duncan: Page 1, "computer aided design (graphical user interface)" Duncan disclosed choosing a subset of resources from a library. Page 12, lines 20-23, "The library of...components can be accessed by the schematic capture package along with a library of schematic components, thereby allowing a circuit design to be created..." Duncan disclosed icons (page 56, lines 6-7), "...a set of basic symbols usable for simple designs will be available." Duncan: Page 1, lines 6-8, "computer-aided design methods for programming programmable integrated circuits (programmable hardware element)...entering a circuit design..." Page 11, line 36-page 12, line 1, "Schematic components include combinatorial circuits and general purpose sequential logic circuits (fixed hardware resources)..." The configurable /programmable hardware element (integrated circuits) and related schematic components are entered using a schematic capture package (Abstract), and displayed on a monitor. Applicant has defined **"fixed hardware resources"** to include (Specification, page 6) **"counters, timers, A/D converters, signal**

conditioning logic, computer interface logic, etc." and (Specification, page 32) **"physical I/O resources such as analog to digital converters (ADCs), digital to analog converters (DACs), and digital lines, among others..."** (emphasis added) Examiner points to the 'underlying circuit design', which is represented as an icon, as a 'fixed hardware resource'.

-receiving user input to the graphical user interface specifying a function;
Duncan disclosed user input at page 12, line 5, "...entering circuit designs into a computer..."

-generating a hardware configuration program based on the user input, wherein the hardware configuration program is deployable on the reconfigurable system;
Duncan disclosed (page 12, lines 31-32), "capture package can translate the state flow diagram (hardware configuration program) to a computer usable form (for example a netlist)..." Page 13, lines 10-13, "...filed programmable gate arrays (FPGAs) ...are programmed..."

Regarding the limitations:
-deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources;
-wherein, after said deploying, the reconfigurable system is operable to perform the function.

Duncan failed to provide specific details related to "deploying" the configuration onto the programmable hardware element. However Wenban disclosed an example of deploying a

hardware configuration (page 36 #2). "A complete FPGA configuration file can be downloaded (deployed) over the network...The other message type is a command that causes the bootstrap loader to reconfigure the FPGA (specifies the use of fixed hardware resource)...The master node can download new application-specific code to be executed on the slave nodes... Page 36, #3 discloses that a slave node (on an embedded token ring network / reconfigurable system) will sample / collect / send (perform the function).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Duncan's invention to provide more explicit details regarding the deployment of programmable code onto a hardware resource, as provided by Wenban because both references are directed towards developing programs to configure hardware. It is inherent that ultimately the program is deployed onto the configurable hardware. Duncan suggested deploying the configuration, (page 13, lines 10-12) "...field programmable gate arrays operable to perform the function)...are programmed in accordance with the present invention...", but Wenban provided a more specific example.

Per claim 3:

-displaying an icon corresponding to the programmable hardware element;

Duncan disclosed (page 12, lines 5-8) symbols (icons) displayed on a computer video terminal by a schematic capture program. Duncan disclosed a (page 12, line 22) "library of schematic components....allowing a circuit design to be created (programmable hardware element)..."

-interactively displaying proposed configurations of the programmable hardware element in response to said receiving user input.

Duncan disclosed displaying proposed configurations in response to user input (page 15, lines 10-11). "...user can modify the contents of the circuit design file until it contains a desired circuit design."

Per claim 4:

Regarding the limitation:

-reconfigurable system is a reconfigurable measurement system, wherein the function is a measurement function.

Broadly, Duncan disclosed the invention produces custom icons to implement the desired circuit design (measurement system). As an example, Duncan disclosed the design of a system for real time compression of a digital video stream. Signal values are measured and selectively compressed.

Per claim 5:

Duncan failed to specifically disclose:

-the reconfigurable system is one or more of a reconfigurable control system, a reconfigurable automation system, and a reconfigurable simulation system;

-wherein the function is a corresponding one or more of a control function, an automation function, and a simulation function, respectively.

However, as an example, Wenban more specifically disclosed (page 34, #10, page 35, #2, #6,

page 36, #6) a digital oscilloscope, range detection using an ultrasonic transducer, and a RIO Processor (reconfigurable control system). Page 35, #2, "The secondary I/O connector supports...real-time integration bus...and may be used to control (function corresponding to control function) commercially available instrumentation cards." Also page 36, #6, "Applications such as robotics and control (control / automation / simulation), which require real-time processing..."

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Duncan's invention to provide more explicit details regarding the control, automation, or simulation systems / functions, as provided by Wenban, because both references are directed towards developing programs to configure hardware. It is well known that configurable hardware is used in control / automation / simulation, especially in embedded hardware. Duncan suggested such an example as video processing (real time processing control), but Wenban provided a more specific examples.

Per claim 6:

-receiving user input regarding one or more of the fixed hardware resources required by an application to perform the function;

Duncan disclosed (page 7, line 35-36) "...user to enter (receiving user input) and edit a circuit design..." Page 11, line 32-page 12, line 1, "...a circuit design includes...schematic components...include combinatorial circuits and general purpose sequential logic circuits,

including counters, registers and flip-flops (fixed hardware resources selected by user as required by application to perform the function)."

-receiving user input specifying timing and triggering requirements of the application with respect to the specified fixed hardware resources.

As an example, Duncan disclosed (page 16, lines 7-27) signal paths connected to clock enable, clock and set terminals of a flip-flop. Various components are provided related to states, such as START (page 15, line 36), ACTIVE (page 16, line 13). State flow components are connected to the schematic components (page 15, lines 4-6) and relate to timing and triggering of the application. Duncan disclosed (page 8, lines 30-32, "The ACTIVATE symbol induces a state to be come active in response to an event (triggering requirement)."

Per claim 7:

-generating a description file which identifies resources and features to perform the function indicated by the user;

Duncan disclosed (page 9, lines 13-18) a schematic editor program which accesses a library (description of resources and features) containing...schematic symbols (identifies resources)...arranged to form a state flow diagram... to produce a single graphical representation of a circuit design. Page 12, lines 15-16, "circuit design which defines the function (perform the function indicated by the user) of the state flow component."

-generating a program from the description file;

Duncan disclosed the creation of a graphical representation (page 9, line 17).

Regarding the limitations:

-generating hardware description language (HDL) code from the program;

-generating the hardware configuration program from the HDL code;

-wherein the hardware configuration program is usable to configure a programmable hardware element comprised in the reconfigurable system to perform the function.

Duncan disclosed generating a program to configure hardware, but failed to specifically disclose HDL code. However, Wenban disclosed (page 33, #7) inputting a list of file names to generate a program, (page 33, #5) linking to generate a program, (page 33, #9, compile into HDL (AHDL) code- "...use Altera's tools to compile the AHDL output of HPC and configure the board (configure a programmable hardware element...to perform the function).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Duncan's invention to provide more explicit details regarding programmatically developing the reconfigurable hardware, as provided by Wenban, because both references are directed towards developing programs to configure hardware. Duncan suggested such an example as (Fig. 5) a netlist generator, which creates a netlist, which in turn produces the programmable logic device configuration. Wenban only provided more details related to the steps in creating and deploying the configurations to a hardware resource.

Per claim 8:

-the program is a graphical program.

Duncan disclosed a (page 1, lines 7-9) computer aided design (graphical program) method for programming programmable integrated circuits. A (page 13, lines 24-30) schematic capture package, including a symbol library is disclosed.

Per claim 9:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

Duncan disclosed programming a FPGA (page 13, lines 10-12). The 'programmable logic device configuration' (Fig. 5, #90) is inherently a program binary file.

Per claim 10:

-executing the hardware configuration program on the programmable hardware element to perform the function;

-wherein said executing comprises: the programmable hardware element executing a first portion of the function;

Duncan disclosed (page 15, lines 7-12) executing the circuit design file.

-the programmable hardware element invoking operation of one or more of the fixed hardware resources to perform a second portion of the function.

As an example, Duncan disclosed (page 50, line 34-page 51, line 2) a test bus that operates to

relay a test value. Another example (page 41-line 27-page 42, line 14) discloses a function (second function portion called) to process data prior to compressing a digital video stream.

Per claim 11:

-displaying a graphical user interface on a display which is useable for configuring the reconfigurable measurement system, wherein the reconfigurable measurement system comprises a programmable hardware element and one or more fixed hardware resources coupled to the programmable hardware element, and wherein the graphical user interface displays icons corresponding to each of at least a subset of the fixed hardware resources;

-receiving user input specifying a measurement function;

-generating a hardware configuration program, wherein the hardware configuration program is deployable on the reconfigurable measurement system;

-deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources;

-wherein, after said deploying, the reconfigurable measurement system is operable to perform the measurement function.

See rejection of limitations as addressed in claims 1 and 4 above.

Per claim 12:

-receiving user input comprises: receiving user input regarding one or more of the fixed hardware resources required by an application to perform the function;

-and receiving user input specifying timing and triggering requirements of the application with respect to the fixed hardware resources.

See rejection of limitations as addressed in claim 6 above.

Per claim 13:

-receiving user input specifying resources required by an application to perform a function, wherein the specified resources comprise one or more fixed hardware resources;

-receiving user input specifying timing and triggering requirements of the application with respect to the specified resources; and generating a hardware configuration program, wherein the hardware configuration program is deployable on the reconfigurable system, wherein, after said deployment, the reconfigurable system is operable to perform the function.

See rejection of limitations as addressed in claims 1 and 6 above.

Per claim 14:

-selecting one or more of hardware and software resources;

Duncan disclosed (page 11, line 31 – page 12, line 1) state flow components (software resources) and schematic components are included in the circuit design invention. Schematic components

(hardware resources) include circuits, counters, registers, etc. Page 13, lines 24-30, discloses a Workview schematic capture package...modified to include Xilinx software which includes symbol library. Page 14, lines 32-33, "The schematic editor is used to enter (user selects resources)..."

-indicating configuration settings for the selected resources.

Duncan disclosed (page 15, line 10) "user can modify the contents of the circuit design file (indicate configuration settings for selected resources)..." Page 15, lines 7-12, "...user can modify the contents (indicate configuration settings for selected resources) of the circuit design file until it contains a desired circuit design."

Per claim 15:

-generating a description file which identifies resources and features indicated by the user;

-generating a program from the description file;

-generating hardware description language (HDL) code from the program;

-generating the hardware configuration program from the HDL code;

-wherein the hardware configuration program is usable to configure a programmable hardware element comprised in the reconfigurable system to perform the function.

See rejection of limitations as addressed in claim 7 above.

Per claim 16:

-the program is a graphical program.

See rejection of limitations as addressed in claim 8 above.

Per claim 17:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

See rejection of limitations as addressed in claim 9 above.

Per claim 18:

-executing the hardware configuration program on the programmable hardware element to perform the function;

-wherein said executing comprises: the programmable hardware element executing a first portion of the function;

-the programmable hardware element invoking operation of one or more of the fixed hardware resources to perform a second portion of the function.

See rejection of limitations as addressed in claim 10 above.

Per claim 19:

-a user computer system accessing the server computer system over a network prior to said receiving user input specifying resources.

Duncan failed to explicitly suggest a server computer system over a network.

However, as an example, Wenban disclosed (page 36, #3) a master / slave (slave accesses server over network) arrangement whereby the master node can download (receiver user inputs specifying resources) oscilloscope code to a slave to perform distributed data collection.

Additionally, see rejection of limitations as addressed in claim 6 above regarding user inputs specifying resources.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Duncan's invention to include server / networking features because Duncan suggested a state machine component that may access external data (page 36, line 35), and the possible inclusion of a test bus (page 51, line 2), both possible uses of a network and server which support use by distributed clients. Graphical user interface software packages meant to configure hardware in remote locations is a cost effective technique for developing / maintaining / updating.

Per claim 20:

-receiving user input specifying a function is performed by a server computer system, the method further comprising:

-a user computer system accessing the server computer system over a network prior to said receiving user input.

See rejection of claim 19 regarding the obvious use of a server computer system and network to optimally configure hardware.

Per claim 21:

A system for configuring a reconfigurable device, comprising:

-a computer system comprising a processor and a memory;

-wherein the memory stores a graphical user interface program which is executable to receive user input specifying a function;

-wherein the memory also stores a configuration generation program which is executable to generate a hardware configuration program based on the user input;

-a device coupled to the computer system, wherein the device includes: a programmable hardware element,

-wherein the hardware configuration program is operable to be deployed onto the programmable hardware element;

-one or more fixed hardware resources coupled to the programmable hardware element;

-wherein the graphical user interface program is further executable to display icons on a display corresponding to each of at least a subset of the fixed hardware resources;

-wherein the hardware configuration program specifies a configuration for the programmable hardware element that implements the function;

-wherein the hardware configuration program further specifies usage of the one or more fixed hardware resources by the programmable hardware element in performing the function;
-wherein, after the hardware configuration program is deployed onto the programmable hardware element, the device is operable to perform the function.

This is a system version of claims 1-10. Duncan disclosed such a 'system'. See Abstract. See rejections of limitations in claims 1, 6, and 7 above.

Per claim 22:

-the graphical user interface program is further executable to modify an appearance of respective fixed hardware resource icons as the corresponding fixed hardware resources are allocated to perform functions in response to the user input,
-wherein the modified appearance of the respective fixed hardware resource icons visually indicates to the user that the corresponding fixed hardware resources have been allocated for use.

See rejection of limitations as addressed in claim 2 above.

Per claim 23:

-the graphical user interface program is further executable to: display an icon corresponding to the programmable hardware element;

-interactively display proposed configurations of the programmable hardware element in response to said receiving user input.

See rejection of limitations as addressed in claim 3 above.

Per claim 24:

-the reconfigurable device is a reconfigurable measurement device, wherein the function is a measurement function.

See rejection of limitations as addressed in claim 4 above.

Per claim 25:

-the reconfigurable device is one or more of a reconfigurable control device, a reconfigurable automation device, and a reconfigurable simulation device;

-wherein the function is a corresponding one or more of a control function, an automation function, and a simulation function, respectively.

See rejection of limitations as addressed in claim 5 above.

Per claim 26:

-receive user input regarding one or more of the fixed hardware resources required by an application to perform the function;

-receive user input specifying timing and triggering requirements of the application with respect to the specified fixed hardware resources.

See rejection of limitations as addressed in claim 6 above.

Per clam 27:

-generate a description file which identifies resources and features to perform the function indicated by the user;

-generate a program from the description file;

-generate hardware description language (HDL) code from the program;

-generate the hardware configuration program from the HDL code;

-wherein the hardware configuration program is usable to configure the programmable hardware element comprised in the reconfigurable device to perform the function.

See rejection of limitations as addressed in claim 7 above.

Per claim 28:

-the program is a graphical program.

See rejection of limitations as addressed in claim 8 above.

Per claim 29:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

See rejection of limitations as addressed in claim 9 above.

Per claim 30:

-the device performing the function comprises the programmable hardware element executing the hardware configuration program to perform the function;

-wherein said executing comprises: the programmable hardware element directly performing a first portion of the function;

-the programmable hardware element invoking operation of one or more of the fixed hardware resources to perform a second portion of the function.

See rejection of limitations as addressed in claim 10 above.

Per claim 31:

A system for configuring a reconfigurable measurement device, comprising:

-a computer system comprising a processor and a memory;

-wherein the memory stores a graphical user interface program which is executable to receive user input specifying a measurement function;

-wherein the memory also stores a configuration generation program which is executable to generate a hardware configuration program based on the user input;

-a device coupled to the computer system, wherein the device includes:

-a programmable hardware element, wherein the hardware configuration program is operable to be deployed onto the programmable hardware element;

-one or more fixed hardware resources coupled to the programmable hardware element;

-wherein the graphical user interface program is further executable to display icons on a display of the computer system corresponding to each of at least a subset of the fixed hardware resources;

-wherein the hardware configuration program specifies a configuration for the programmable hardware element that implements the measurement function;

-wherein the hardware configuration program further specifies usage of the one or more fixed hardware resources by the programmable hardware element in performing the measurement function;

-wherein, after the hardware configuration program is deployed onto the programmable hardware element, the measurement device is operable to perform the measurement function.

This is a system version of claims 1-10. See rejection of limitations as addressed in claims 1 and 4 above.

Per claim 32:

-a deployment program executable to deploy the hardware configuration program onto the

programmable hardware element, wherein, after said deployment, the programmable hardware element is operable to perform the measurement function in conjunction with the one or more fixed hardware resources.

See rejection of limitations as addressed in claims 1 and 4 above.

Per claim 33:

A system for configuring a reconfigurable device, comprising:

-a computer system comprising a processor and a memory, wherein the memory stores a graphical user interface program which is executable to:

Duncan disclosed a processor and a memory (page 13, lines 37) storing a graphical user interface program.

-receive user input specifying resources required by an application to perform a function, wherein the resources comprises one or more fixed hardware resources;

-receive user input specifying timing and triggering requirements of the application with respect to the specified resources;

-wherein the memory also stores a configuration generation program which is executable to:

-generate a hardware configuration program, wherein the hardware configuration program is deployable on the reconfigurable system,

-wherein, after said deployment, the reconfigurable device is operable to perform the function;

-a reconfigurable device coupled to the computer system, wherein the device includes:

-a programmable hardware element, wherein the hardware configuration program is operable to be deployed onto the programmable hardware element;

-one or more resources, comprising the one or more fixed hardware resources, coupled to the programmable hardware element;

-wherein the graphical user interface program is further executable to display icons on a display of the computer system corresponding to each of at least a subset of the resources;

-wherein the hardware configuration program specifies a configuration for the programmable hardware element that implements the function;

-wherein the hardware configuration program further specifies usage of the one or more resources by the programmable hardware element in performing the function;

-wherein, after the hardware configuration program is deployed onto the programmable hardware element, the device is operable to perform the function.

This is a system version of claims 1-10. See rejection of limitations as addressed in claims 1, 6, and 7 above.

Per claim 34:

-specifying resources comprises: selecting one or more of hardware and software resources;

-indicating configuration settings for the selected resources.

See rejection of limitations as addressed in claim 14 above.

Per claim 35:

-generate a description file which identifies resources and features indicated by the user;

-generate a program from the description file;

-generate hardware description language (HDL) code from the program;

-generate the hardware configuration program from the HDL code;

-wherein the hardware configuration program is usable to configure a programmable hardware element comprised in the reconfigurable system to perform the function.

See rejection of limitations as addressed in claim 7 above.

Per claim 36:

-the program is a graphical program.

See rejection of limitations as addressed in claim 8 above.

Per claim 37:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

See rejection of limitations as addressed in claim 9 above.

Per claim 38:

-graphical user interface program is executed on a server computer system;

-wherein said user input specifying resources is received from a user computer system accessing the server computer system over a network.

See rejection of limitations as addressed in claims 19 and 20 above.

Per claim 39:

-graphical user interface program is executed on a server computer system;

-wherein said user input specifying resources and said user input specifying timing and triggering requirements are received by a user computer system accessing the server computer system over a network.

See rejection of limitations as addressed in claim 20 above.

Per claim 40:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

See rejection of limitations as addressed in claim 9 above.

Per claim 41:

A memory medium comprised on a computer system, comprising:

-a graphical user interface program which is executable to receive user input specifying a function;

-a configuration generation program which is executable to generate a hardware configuration program based on the user input;

-wherein said hardware configuration program is usable to configure a device coupled to the computer system, wherein the device includes:

-a programmable hardware element, wherein the hardware configuration program is operable to be deployed onto the programmable hardware element;

-one or more fixed hardware resources coupled to the programmable hardware element;

-wherein the graphical user interface program is further executable to display icons on a display corresponding to each of at least a subset of the fixed hardware resources;

-wherein the hardware configuration program specifies a configuration for the programmable hardware element that implements the function;

-wherein the hardware configuration program further specifies usage of the one or more fixed hardware resources by the programmable hardware element in performing the function;

-wherein, after the hardware configuration program is deployed onto the programmable hardware element, the device is operable to perform the function.

This is a 'memory medium comprised on a computer system' version of claims 1-10 above. See rejection of limitations as addressed in claim 1 above. Duncan disclosed a "memory medium" on a computer system at page 13, line 34.

Per claim 42:

-the graphical user interface program is further executable to modify an appearance of respective fixed hardware resource icons as the corresponding fixed hardware resources are allocated to perform functions in response to the user input,

-wherein the modified appearance of the respective fixed hardware resource icons visually indicates to the user that the corresponding fixed hardware resources have been allocated for use.

See rejection of limitations as addressed in claim 2 above.

Per claim 43:

-display an icon corresponding to the programmable hardware element;

-interactively display proposed configurations of the programmable hardware element in response to said receiving user input.

See rejection of limitations as addressed in claim 3 above.

Per claim 44:

-the reconfigurable device is a reconfigurable measurement device, wherein the function is a

measurement function.

See rejection of limitations as addressed in claim 4 above.

Per claim 45:

-the reconfigurable device is one or more of a reconfigurable control device, a reconfigurable automation device, and a reconfigurable simulation device;

-wherein the function is a corresponding one or more of a control function, an automation function, and a simulation function, respectively.

See rejection of limitations as addressed in claim 5 above.

Per claim 46:

-receive user input regarding one or more of the fixed hardware resources required by an application to perform the function;

-receive user input specifying timing and triggering requirements of the application with respect to the specified fixed hardware resources.

See rejection of limitations as addressed in claim 6 above.

Per claim 47:

-generate a description file which identifies resources and features to perform the function indicated by the user; generate a program from the description file;

-generate hardware description language (HDL) code from the program;

-generate the hardware configuration program from the HDL code;

-wherein the hardware configuration program is usable to configure the programmable hardware element comprised in the reconfigurable device to perform the function in conjunction with the one or more fixed hardware resources.

See rejection of limitations as addressed in claim 7 above.

Per claim 48:

-the program is a graphical program.

See rejection of limitations as addressed in claim 8 above.

Per claim 49:

-a deployment program executable to deploy the hardware configuration program onto the programmable hardware element, wherein, after said deployment, the programmable hardware element is operable to perform the function in conjunction with the one or more fixed hardware resources.

See rejection of limitations as addressed in claims 1 and 10 above.

Per claim 50:

-the programmable hardware element is a field programmable gate array (FPGA), and wherein the hardware configuration program comprises a program binary file for the FPGA.

See rejection of limitations as addressed in claim 9 above.

7. Claims 2, 22, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 94/15311 to Duncan (submitted as IDS on 10/06/2004) (hereinafter Duncan), in view of "A Software Development System for FPGA-Based Data Acquisition Systems" by Alan Wenban and Geoffrey Brown (hereinafter Wenban), and further in view of US Patent 5,005,119 to Rumbaugh et al.

Per claims 2, 22, and 42:

Duncan / Wenban disclosed a graphical user interface to develop code for configurable hardware resources (Duncan, page 13, lines 24-37). Duncan / Wenban failed to disclose:

-modifying an appearance of respective fixed hardware resource icons as the corresponding fixed hardware resources are allocated to perform functions in response to the user input, wherein the modified appearance of the respective fixed hardware resource icons visually indicates to the

user that the corresponding fixed hardware resources have been allocated for use.

However, Rumbaugh disclosed a CAD design program (graphical user interface development program) whereby users select icons for code development. Col. 12, lines 18-32, "...the...program acknowledges the user selection by highlighting the icon of the selected data token such as by changing its color.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify the Duncan / Wenban invention, by including "modifying an appearance of a resource icon" as it is selected by a user, as disclosed by Rumbaugh, because such a visual indicator makes programming more intuitive to a user. All references are directed towards a (Rumbaugh, col. 1, line 11) computer-aided engineering design environment. Duncan, col. 2, lines 38-44: Such design features provide tools to assist in the design process in a user friendly fashion.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei

Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned: 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman 

05/23/2006